DETAILED ACTION

1. Claims 1-21 are pending.

Papers Filed

2. Examiner acknowledges receipt of remarks and amended claims, filed on 10 July 2008.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-21 and 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Strombergson (U.S. Patent No. 6,807,621) in view of Harris (U.S. Patent No. 6,260,138).

3. As per claim 1, Strombergson discloses a device comprising:

a first device (Fig. 1 reservation unit 3A in combination with execution unit 4A) to track segment order associated with a first execution unit (Fig. 1 execution unit 4A);

a second device (Fig. 1 reservation unit 3B in combination with execution unit 4B) to track segment order associated with a second execution unit (Fig. 1 execution unit 4B); *The examiner asserts that a single instruction constitutes a segment of the program running on Strombergson's processor. Further, the examiner asserts that the*

reservation unit 3A/B receives instructions intended for execution unit 4A/B. The reservation unit tracks instructions. Col. 4 lines 45-51 dictate that instructions are checked for irregularities in the order that they were received at the decode stage. The reservation unit must inherently track instruction order if it is to check for irregularities in the proper order.

and a third device (Fig. 1 commit stage 5 in combination with switch point storing registers) coupled to the first device and second device to track relative segment order between the first device and the second device. *The examiner asserts that the commit stage is coupled to the first and second execution and reservation units as pictured in Fig. 1. Further, the reorder buffer must track instructions through all execution units. If the reorder buffer did not keep track of instruction order, instructions would not be guaranteed to complete in the proper order, causing undesired operation of the processor.*

Strombergson discloses identifying instructions that are required to be flushed during a mispredicted branch (col 2 lines 14-23), but fails to disclose that these instructions are among consecutive sets of instructions with a switch point indicating a transition from a first to a second reorder buffer.

Harris discloses instruction path separated by conditional branch instructions, where different branch paths are sent to different execution units (fig. 6 and col 7 lines 9-37)

Strombergson would have been motivated to utilize this technique to increase the throughput of the processor, simplify recovery for mispredictions, and not suffer the same fallbacks associated to prior art Figs. 2-4.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Strombergson and allow the conditional branch instructions to be separated into branch paths that are given separate execution units (and, in accordance with Strombergson fig. 1, separate reorder buffers).

4. As per claim 2, Strombergson/Harris discloses the device of claim 1, wherein the first device (Fig. 1 reservation unit 3A in combination with execution unit 4A) is operable to notify the third device (Fig. 1 commit stage 5) of a mispredicted instruction in a segment, and wherein the first device is operable to flush a first segment. (Col. 3 lines 34-60)

5. As per claim 3, Strombergson/Harris discloses the device of claim 2, wherein the third device (Fig. 1 commit stage 5) is operable to notify the second device (Fig. 1 reservation unit 3B in combination with execution unit 4B) of the mispredicted instruction in the segment, and wherein the second device is operable to flush a second segment. (Col. 3 lines 34-60)

6. As per claim 4, Strombergson/Harris discloses the device of claim 2, wherein the third device (Fig. 1 commit stage 5) is operable to notify the first device (Fig. 1

reservation unit 3A in combination with execution unit 4A) of the mispredicted instruction in the segment, and wherein the first device is operable to flush a third segment. (Col. 3 lines 34-60)

7. As per claim 5, Strombergson/Harris discloses the device of claim 1, further comprising: a fetch control unit (Fig. 1 fetch unit 1 in combination with decode unit 2) to predict segment order (Col. 4 line 57-58), fetch segments and assign the segments to one of the first device and the second device during a flush operation. (Col. 7 lines 42-54)

8. As per claim 6, Strombergson/Harris discloses a method comprising:

tracking the program order of a first set of instructions assigned to a first local reorder buffer (Fig. 1 reservation unit 3A in combination with execution unit 4A) in a first execution unit (Fig. 1 reservation unit 3A in combination with execution unit 4A);

tracking the program order of a second set of instructions assigned to a second local reorder buffer (Fig. 1 reservation unit 3B in combination with execution unit 4B) in a second execution [unit] (Fig. 1 reservation unit 3B in combination with execution unit 4B);

and tracking program order of the first set of instructions relative to the second set of instructions in a global reorder buffer (Fig. 1 commit stage 5). *The examiner asserts that since the commit stage contains a reorder buffer (ROB*

10), the stage is responsible to for tracking program order from all the execution stages.

9. As per claim 7, Strombergson/Harris discloses the method of claim 6, further comprising:

notifying the global reorder buffer (Fig. 1 commit stage 5) when a mispredicted instruction occurs; (Col. 3 lines 34-60)

intiating a flush operation in the global reorder buffer (Fig. 1 commit stage 5); (Col. 3 lines 34-60)

and notifying the first local reorder buffer (Fig. 1 reservation unit 3A in combination with execution unit 4A) of the mispredicted instruction. (Col. 3, lines 34-60)

10. As per claim 8, Strombergson/Harris discloses the method of claim 7, further comprising: notifying a fetch control unit (Fig. 1 fetch unit 1 in combination with decode unit 2) of a mispredicted set of instructions. (Col. 3 line 51)

11. As per claim 9, Strombergson/Harris discloses the method of claim 6, further comprising: sending a signal to the second local reorder buffer (Fig. 1 reservation unit 3B in combination with execution unit 4B) to flush at least a third set of instructions. (Col. 3 line 58-60)

12. As per claim 10, Strombergson/Harris discloses the method of claim 6, further comprising: fetching a fourth set of instructions; and assigning the fourth set of instruction to the first reorder buffer during a flushing operation. *The examiner asserts that the processor will continue to process instructions, starting with the branch target instruction, after a conditional branch has been taken. These instructions will be issued to the functional stages, including the stage including the first reorder buffer, and will be executed once the flushing of the stage has been completed.*

13. As per claim 11, Strombergson/Harris discloses the method of claim 6, further comprising: retiring an instruction according to an indicator stored in the global reorder buffer(Fig. 1 commit stage 5). (Col. 8 lines 22-27) *The examiner asserts that indicators must exist to reorder instructions after execution.*

14. As per claim 12, Strombergson/Harris discloses a system comprising:

a bus; (Fig. 1, line connecting memory 7 to fetch unit 1)

a memory device coupled to the bus; (Fig. 1 memory 7)

and a processor including a fetch control unit (Fig. 1 fetch unit 1 and decode unit 2) to fetch instructions from the memory device, a first execution unit (Fig. 1 reservation unit 3A in combination with execution unit 4A) to process one or more of the fetched instructions, a second execution unit (Fig. 1 reservation unit 3B in combination with execution unit 4B) to process one of more of the fetched instructions, a first reorder buffer (Fig. 1 reservation unit 3A in

combination with execution unit 4A) to track instructions assigned to the first execution unit, a second reorder buffer (Fig. 1 reservation unit 3B in combination with execution unit 4B) to track instructions assigned to the second execution unit, and a global reorder buffer (Fig. 1 commit stage 5) to track instruction order of instructions assigned to the first reorder buffer relative to the second reorder buffer. (Col. 8 lines 22-27) *The examiner asserts that the reservation station in combination with the execution unit track a given instruction as it waits to be, and is finally executed. The examiner asserts that the reorder buffer 10 in commit stage 5 tracks the order of instructions as it retires instructions in their proper order.*

By storing data for a set of switch points, the data indicating a transition in assignment of consecutive sets of instructions from the first reorder buffer to the second reorder buffer, the global reorder buffer to identify a switch point from the set of switch points that is associated with an instruction occurring after a mispredicted instruction (Harris Fig. 6 and col7 lines 9-37).

15. As per claim 13, Strombergson/Harris discloses the system of claim 12, wherein the first reorder buffer is operable to signal the global reorder buffer upon detection of a mispredicted instruction. (Col. 3 lines 34-60)

16. As per claim 14, Strombergson/Harris discloses the system of claim 12, wherein the first reorder buffer is operable to flush a first set of instructions upon detection of a mispredicted instruction (Col. 3 lines 34-60), and wherein the fetch control unit assigns

a second set of instructions to the first reorder buffer based on a set of load balancing criteria. *The examiner asserts that the processor will continue to process instructions, starting with the branch target instruction, after a conditional branch has been taken. These instructions will be issued to the functional stages, including the stage including the first reorder buffer, and will be executed once the flushing of the stage has been completed.*

17. As per claim 15, Strombergson/Harris discloses a machine readable medium having stored therein instructions, which when executed cause a machine to perform a set of operations comprising:

tracking the program order of a first set of instructions assigned to a first local tracking device in a first execution unit (Fig. 1 reservation unit 3A in combination with execution unit 4A); *The examiner asserts that the reservation station in combination with the execution unit track a given instruction as it waits to be, and is finally executed.*

tracking the program order of a second set of instructions assigned to a second local tracking device in a second execution unit (Fig. 1 reservation unit 3B in combination with execution unit 4B); *The examiner asserts that the reservation station in combination with the execution unit track a given instruction as it waits to be, and is finally executed.*

and tracking program order of the first set of instructions relative to the second set of instructions in a global tracking device. (Fig. 1 commit stage 5) *The*

examiner asserts that the reorder buffer 10 in commit stage 5 tracks the order of instructions as it retires instructions in their proper order.

Bye storing data for a set of switch points, the data indicating a transition in assignment of consecutive sets of instructions from the first reorder buffer to the second reorder buffer, the global reorder buffer to identify a switch point from the set of switch points that is associated with an instruction occurring after a mispredicted instruction (Harris Fig. 6 and col7 lines 9-37).

18. As per claim 16, Strombergson/Harris discloses the machine readable medium of claim 15, having further instructions stored therein which when executed cause a machine to perform a set of operations further comprising: notifying the global tracking device (Fig. 1 commit stage 5) when a mispredicted instruction occurs. (Col. 3 line 55-57)

19. As per claim 17, Strombergson/Harris discloses the machine readable medium of claim 16, having further instructions stored therein which when executed cause a machine to perform a set of operations further comprising: tracking a first set of switch points in the global tracking device (Fig. 1 commit stage 5). *The examiner further asserts that the reorder buffer 10 tracks a given instruction compared to prior and subsequent instructions to maintain proper instruction ordering.*

20. As per claim 18, Strombergson/Harris discloses the machine readable medium of claim 16, having further instructions stored therein which when executed cause a machine to perform a set of operations further comprising: flushing a second set of switch points based on the mispredicted instruction. *The examiner asserts that when a conditional branch instruction is mispredicted, instructions currently in other stages of the pipeline are flushed as described in col. 3 lines 34-60.*

21. As per claim 19, Strombergson/Harris discloses an apparatus comprising:

a means for tracking the program order of a first set of instructions assigned to a first local tracking device (Fig. 1 reservation unit 3A in combination with execution unit 4A) in a first execution unit (Fig. 1 reservation unit 3A in combination with execution unit 4A); *The examiner asserts that the reservation station in combination with the execution unit track a given instruction as it waits to be, and is finally executed.*

a means for tracking the program order of a second set of instructions assigned to a second local tracking device (Fig. 1 reservation unit 3B in combination with execution unit 4B) in a second execution unit (Fig. 1 reservation unit 3B in combination with execution unit 4B); *The examiner asserts that the reservation station in combination with the execution unit track a given instruction as it waits to be, and is finally executed.*

and a means for tracking program order of the first set of instructions relative to the second set of instructions in a global tracking device. (Fig. 1

commit stage 5) *The examiner asserts that the reorder buffer 10 in commit stage 5 tracks the order of instructions as it retires instructions in their proper order.*

By storing data for a set of switch points, the data indicating a transition in assignment of consecutive sets of instructions from the first reorder buffer to the second reorder buffer, the global reorder buffer to identify a switch point from the set of switch points that is associated with an instruction occurring after a mispredicted instruction (Harris Fig. 6 and col7 lines 9-37).

22. As per claim 20, Strombergson/Harris discloses the apparatus of claim 19, further comprising: a means for notifying the global tracking device when a mispredicted instruction occurs. (Col. 3 lines 34-60)

23. As per claim 21, Strombergson/Harris discloses the apparatus of claim 19, further comprising: a means for flushing at least a third set of instructions in the first local tracking device. (Col. 3 lines 34-60)

24. Regarding claims 27-31, Strombergson/Harris discloses the devices/methods of claims 1, 6, 12, 15 and 19 further comprising: maintaining a segment preceding the mispredicted instruction in response to a remote flush operation received from the global reorder buffer (Harris col 7 line 44 to col 8 line 5).

Response to Arguments

Applicant's arguments filed 08 January 2008 have been fully considered but they are not persuasive.

Applicant's amendments are fully disclosed in the referenced provided. In particular, the amendment to the independent claims requires "the first device to identify and flush a segment that is subsequent to a switch point." Applicant states that "Harris is silent regarding flushing segments or instructions." This statement is untrue. Harris does not use the term "flush"; Harris uses the term "annulled." It is perfectly clear from column 7 line 44 to col 8 line 5 that not only are both instruction paths taken during a branch prediction, but the improper path is flushed (annulled). The portion of the system completing this flush is considered to be, for example, within the definition of "third device" with respect to the rejection of claim 1. The other independent claims have similar interpretations. Similarly, since the correct path is not annulled, the new limitations of claims 27-31 are satisfied. It follows that one of the segments (the correct one) is maintained after the remote flush instruction has been received.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Brian Johnson/ 2183 Patent Examiner

/Eddie P Chan/

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